**Amendments to the Claims**

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1. (currently amended) A graphics rendering engine stored on a computer-storage medium and executable by a computer, the graphics rendering engine comprising:

a sequence of instruction addresses ~~adapted~~ for display upon a screen ~~that is~~ accessible to a user, wherein the screen comprises a graphical user interface (GUI) for receiving user input to select one of the instruction addresses;

a sequence of processor pipeline stages attributable to respective ones of the ~~sequence of~~ instruction~~s and~~ addresses, wherein during times when ~~a~~ the user ~~selects one of the instruction addresses~~ input is received by the GUI, the screen displays:

a designator for at least one of the instruction~~s~~ addresses to denote ~~the~~ that a corresponding designated instruction address will proceed to a succeeding stage in the processor pipeline during a next clock cycle; and

a non-designator for another one of at least one of the instruction~~s~~ addresses to denote ~~the~~ that a corresponding non-designated instruction address will not proceed to a succeeding stage in the processor pipeline during the next clock cycle.

2. (canceled)

3. (original) The graphics rendering engine as recited in claim 1, wherein the screen comprises a pop-up window.

4. (original) The graphics rendering engine as recited in claim 1, wherein the designator is a color that highlights the stage attributable to the at least one instruction that will proceed to the succeeding stage.

5. (original) The graphics rendering engine as recited in claim 4, wherein the color differs depending on which stage is highlighted.

6. (currently amended) The graphics rendering engine as recited in claim 1, wherein the processor pipeline is a pipeline of a ~~supserscalar~~ superscalar processor where more than one instruction can exist within each stage of the pipeline.

7. (currently amended) The graphics rendering engine as recited in claim 1, wherein the user actuates a pointing device to ~~select~~ supply the user input to the GUI for selecting only one of the instruction addresses ~~and~~, wherein in response ~~thereto~~ to said selection, the screen displays ~~a~~ the designator over ~~the~~ a field bearing ~~the~~ a stage name for all of the ~~sequence of instructions~~ instruction addresses that will proceed to the next stage in the processor pipeline ~~sequence~~.

8. (currently amended) A software development tool stored on a computer-storage medium and executable by a computer, the software development tool comprising:

source code represented as a first sequence of instruction addresses;

a graphics rendering engine coupled to receive the first sequence of instruction addresses and produce a graphical user interface (GUI) window that includes:

a breakpoint field that, upon receiving user input via a pointing device:

selects a particular instruction address within the first sequence of instruction addresses shown in a particular stage of a processor pipeline;

displays all instruction addresses within the first sequence of instruction ~~address~~ addresses along with corresponding stages of the processor pipeline during a clock cycle in which the particular instruction address is within the particular stage;

assigns a designator to at least one instruction address of the first sequence of instruction addresses to denote ~~the~~ that a corresponding designated instruction will proceed to a succeeding stage in the ~~micro~~processor pipeline during a clock cycle succeeding the clock cycle; and

assigns a non-designator to another at least one instruction address of the first sequence of instruction addresses to denote that a corresponding non-designated instruction will not proceed to a succeeding stage in ~~within~~ the ~~micro~~processor pipeline during a clock cycle succeeding the clock cycle;

an instruction address field that, upon selection by a user via the pointing device, allows the user to move said another at least one instruction address; and

a scheduler that responds to the moved said another at least one instruction address to form a second sequence of instruction~~s~~ addresses that has a higher instruction throughput in the processor pipeline than the first sequence of ~~instructions~~ instruction addresses.

9. (currently amended) The software development tool as recited in claim 8, wherein the graphics rendering engine further displays all instructions within the first sequence of ~~instructions~~ instruction addresses and assigns a designator to a number of the instruction ~~address~~ addresses of the second sequence of ~~instructions~~ instruction addresses that ~~exceed~~ exceeds a number of the at least one instruction ~~address~~ addresses of the first sequence of instruction addresses.

10. (currently amended) The software development tool as recited in claim 8, wherein the second sequence of ~~instructions~~ instruction addresses requires fewer clock cycles through the processor pipeline than the first sequence of ~~instructions~~ instruction addresses.

11. (original) The software development tool as recited in claim 8, wherein the window comprises a pop-up window rendered upon a computer display screen.

12. (currently amended) The software development tool as recited in claim 8, wherein the designator is a color that highlights the stage attributable to the at least one instruction address that will proceed to the succeeding stage.

13. (original) The software development tool as recited in claim 12, wherein the color differs depending on which stage is highlighted.

14. (currently amended) The software development tool as recited in claim 8, wherein the processor pipeline is a pipeline of a ~~supserscalar~~ superscalar processor where more than one instruction can exist within each stage of the pipeline.

15. (currently amended) The software development tool as recited in claim 8, wherein the user actuates ~~a~~ the pointing device to select ~~only one of~~ the particular instruction ~~addresses~~ address and, in response thereto, the window displays ~~a~~ the designator over a stage number field bearing ~~the~~ a stage name for all of the first sequence of ~~instructions~~ instruction addresses that will proceed to the ~~next~~ succeeding stage in the processor pipeline ~~sequence~~.

16. (currently amended) A method for displaying progression of instruction addresses through a processor pipeline, comprising:

selecting a breakpoint within a breakpoint column of a display screen, via user input at a breakpoint location on the display screen, to select:

an instruction address within the same line as the breakpoint[[,]]; and

a clock cycle associated with the selected instruction address being in a stage within the processor pipeline;

designating all instruction addresses within the processor pipeline that will proceed to ~~the~~ a succeeding stage of the processor pipeline; and

not designating all instruction addresses within the processor pipeline that will not proceed to ~~the~~ a succeeding stage of the processor pipeline.

17. (currently amended) The method as recited in claim 16, wherein said designating comprises receiving a signal from a stage debug register by a graphics rendering engine to denote that the instruction addresses being designated will proceed to the ~~next~~ succeeding stage of the processor pipeline.

18. (original) The method as recited in claim 16, wherein said designating comprises checking resources of a processor to determine if the instruction addresses will be allowed to proceed and, if so, sending a signal from a debug register that stores the checking outcome to designate the instruction addresses that have corresponding resources available to allow such instruction addresses to proceed.

19. (currently amended) The method as recited in claim 16, wherein said designating comprises highlighting the designated instruction addresses with a color different from the background color of the display screen.

20. (currently amended) The method as recited in claim 16, wherein said designating comprises highlighting the stage corresponding to the designated instruction addresses with a color, and wherein the color differs depending on which stage is highlighted.